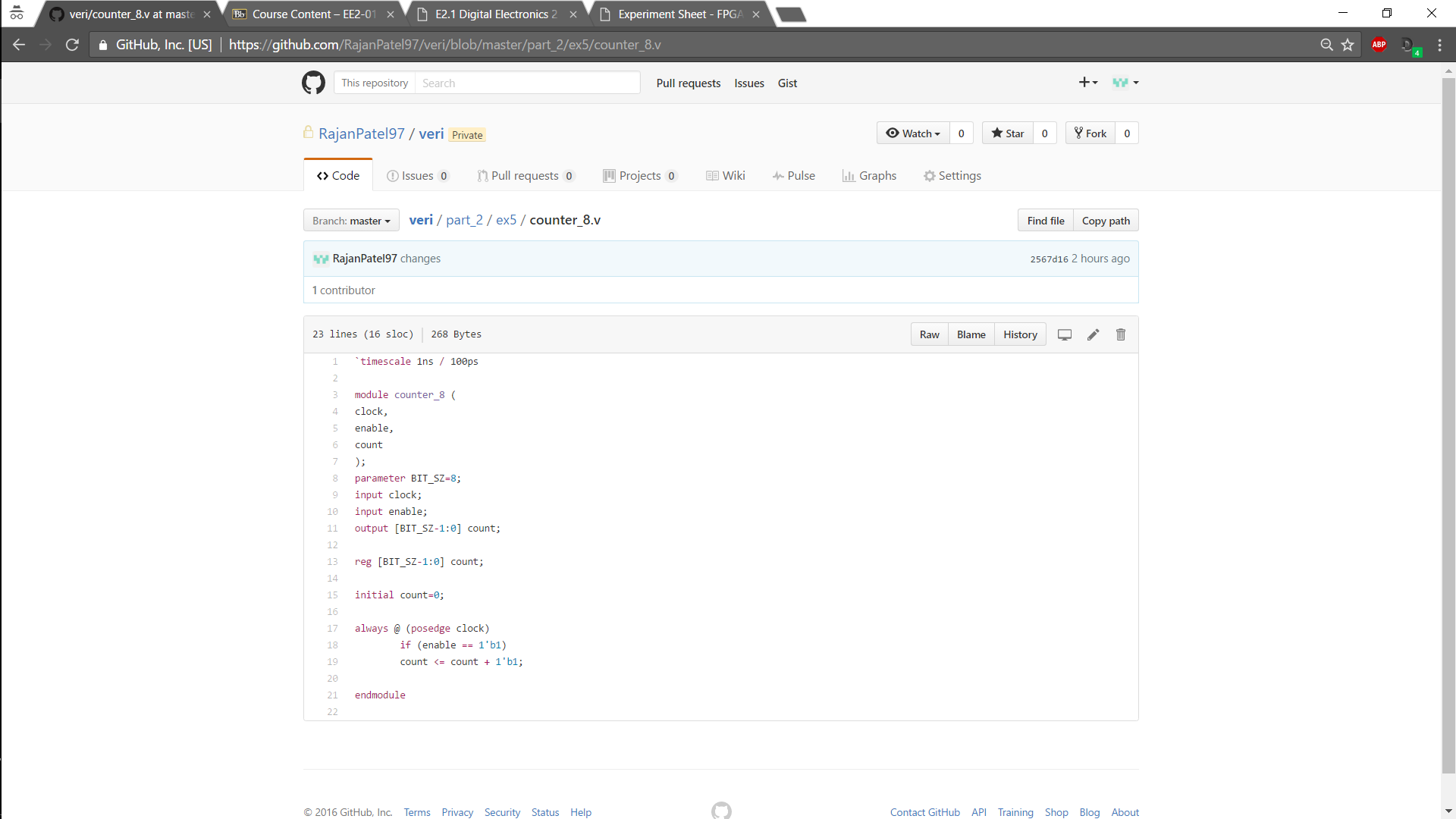
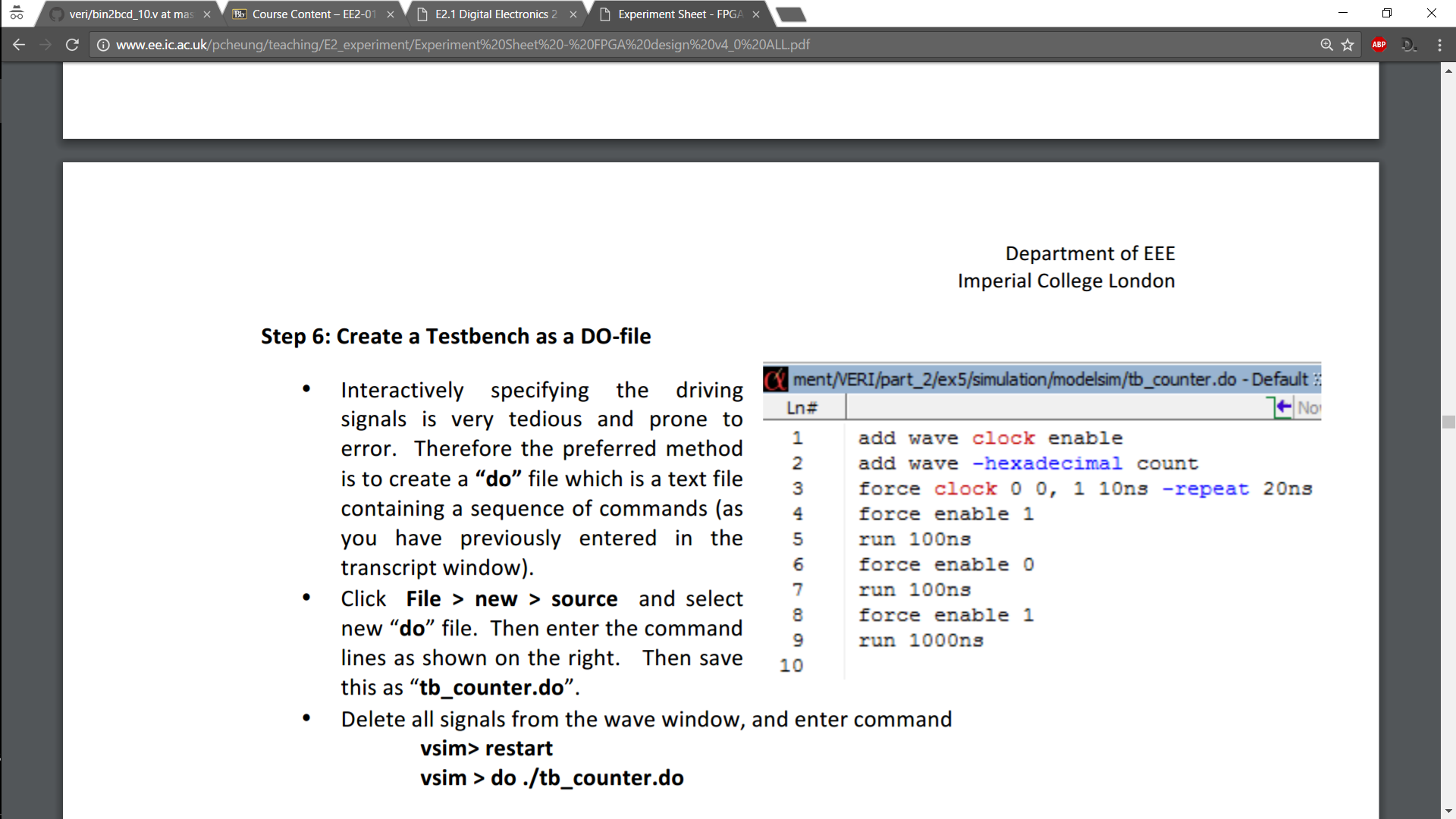
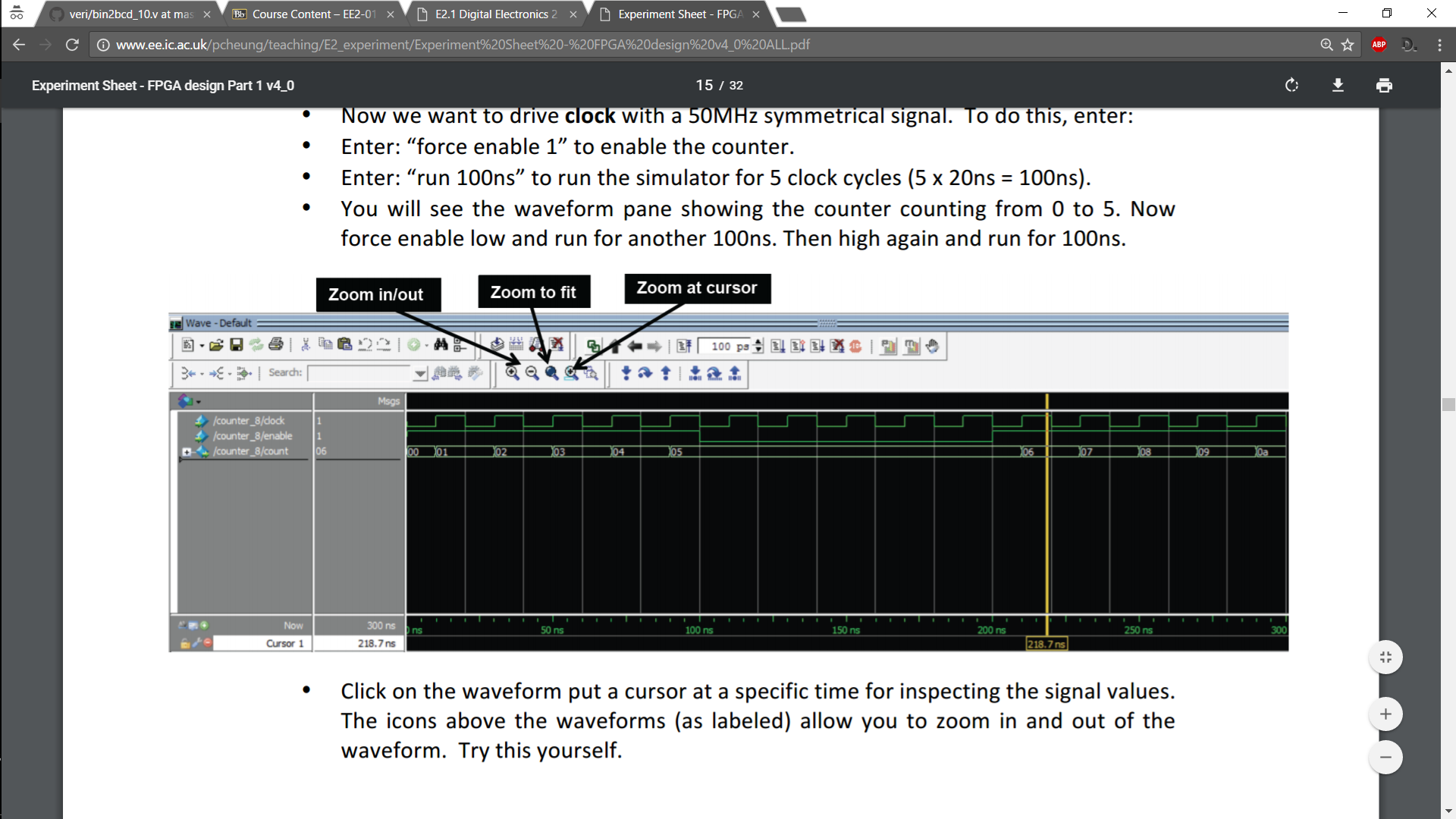
Verilog Experiment - Part 2

Experiment 5

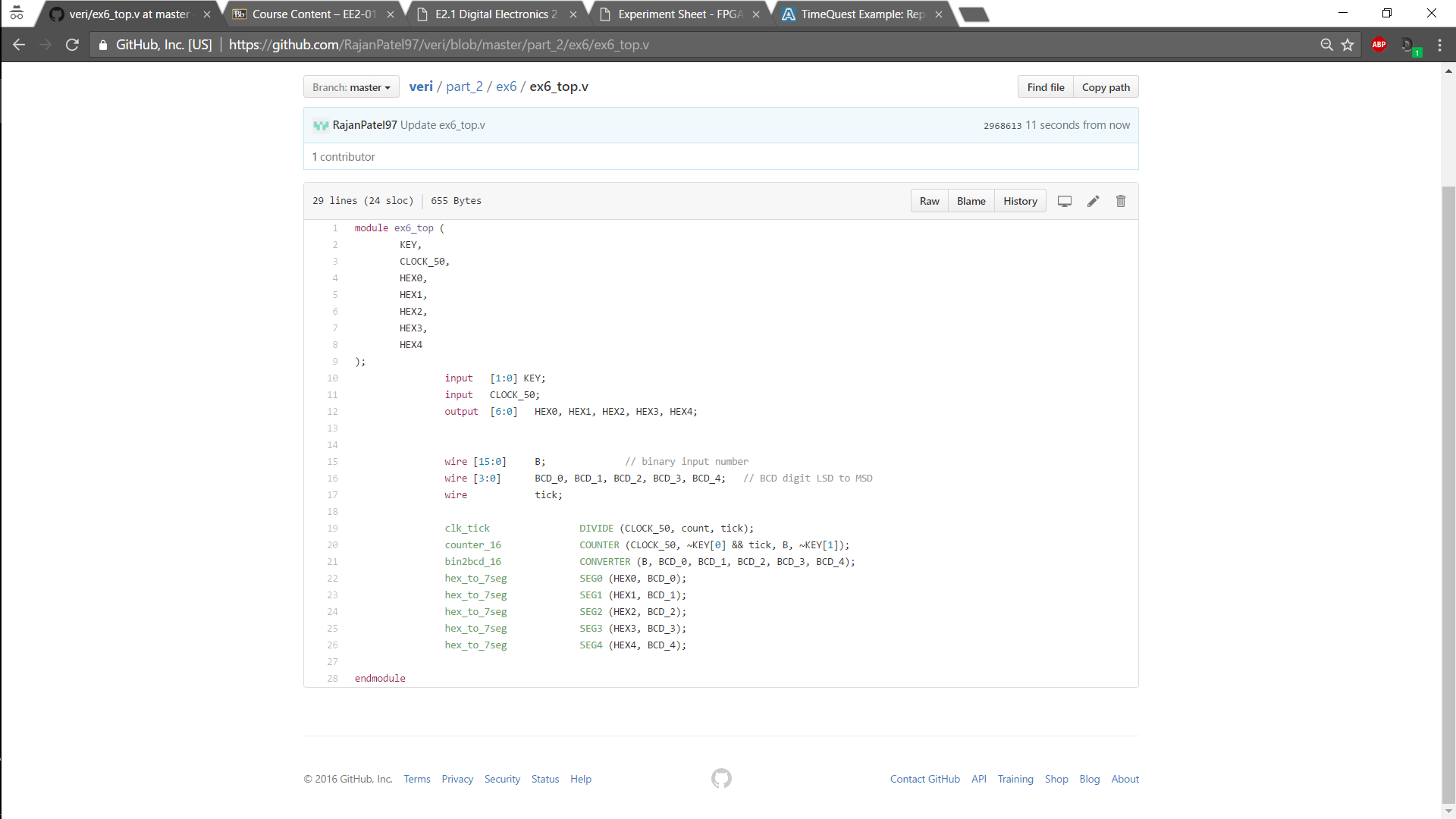


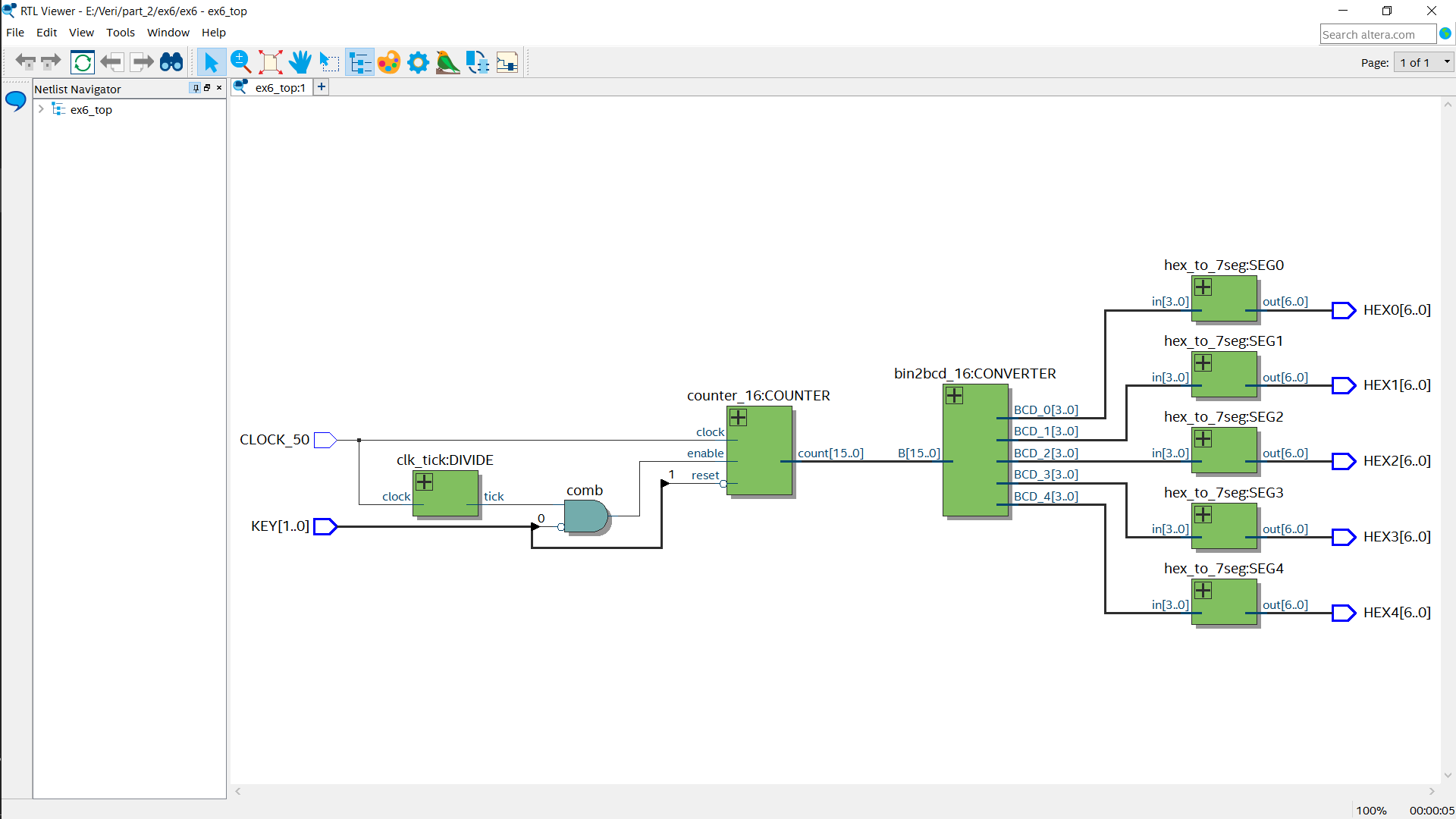


Experiment 6

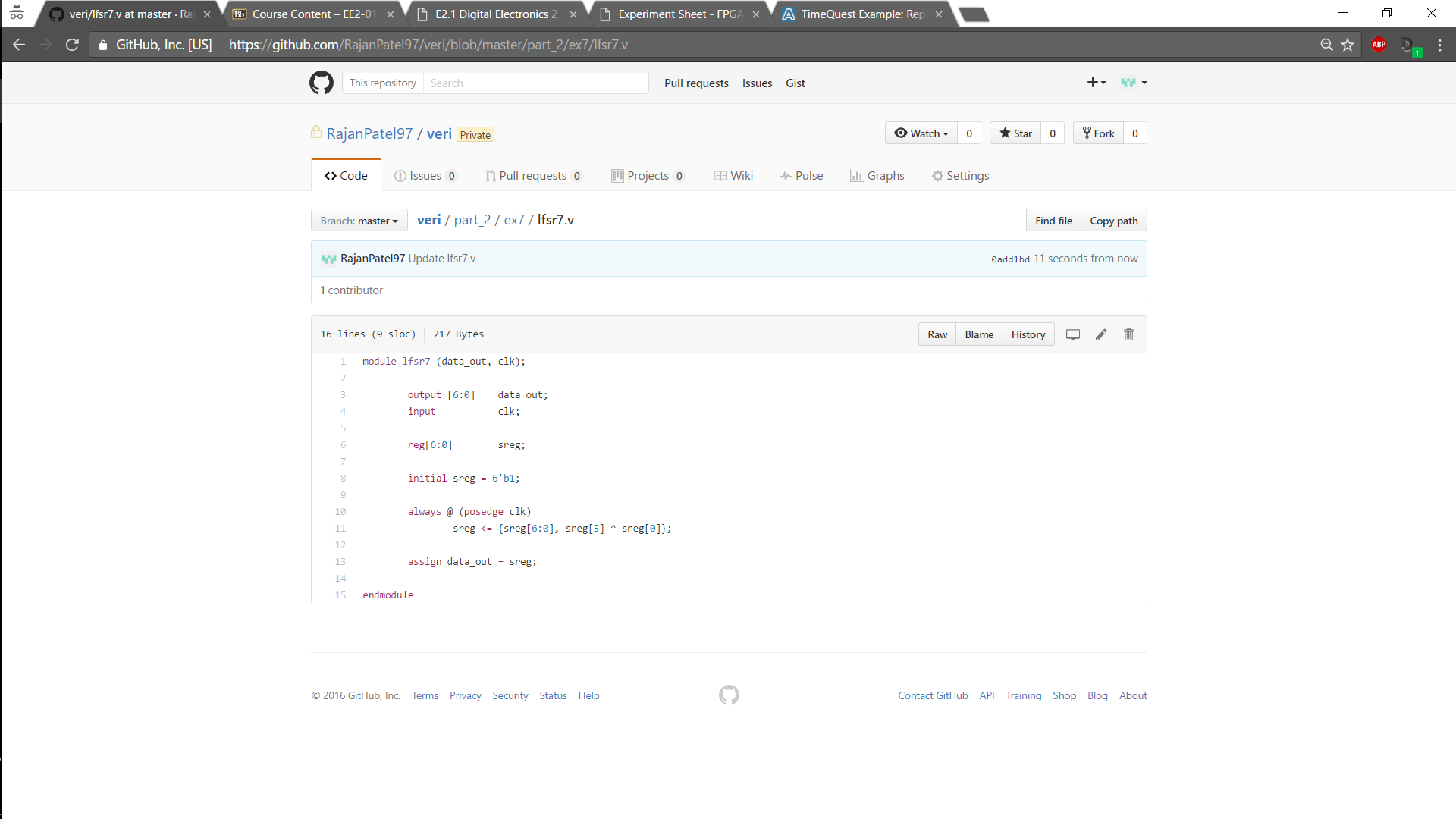
445.04 MHz - 85

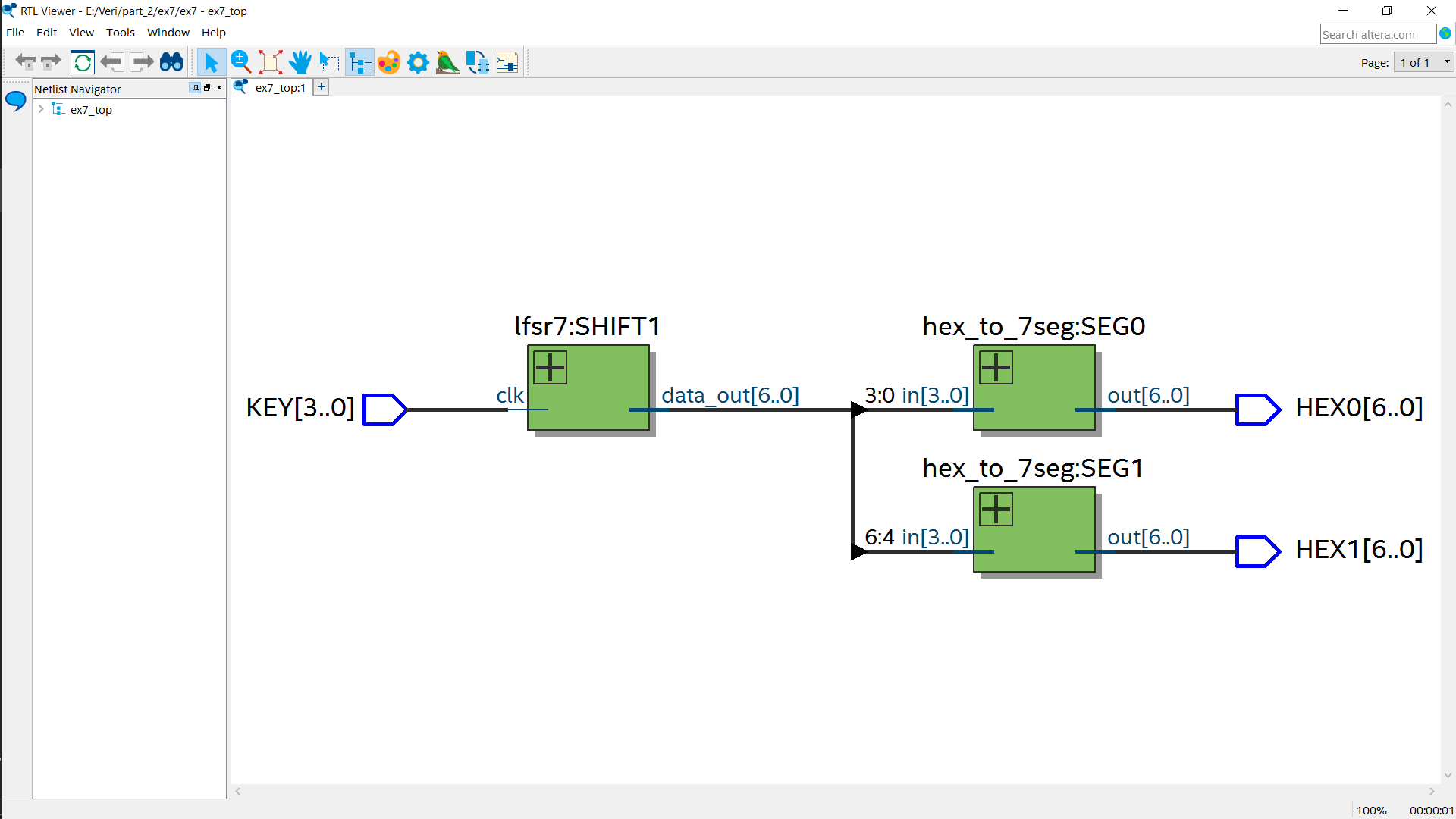
422.48 MHz - 0

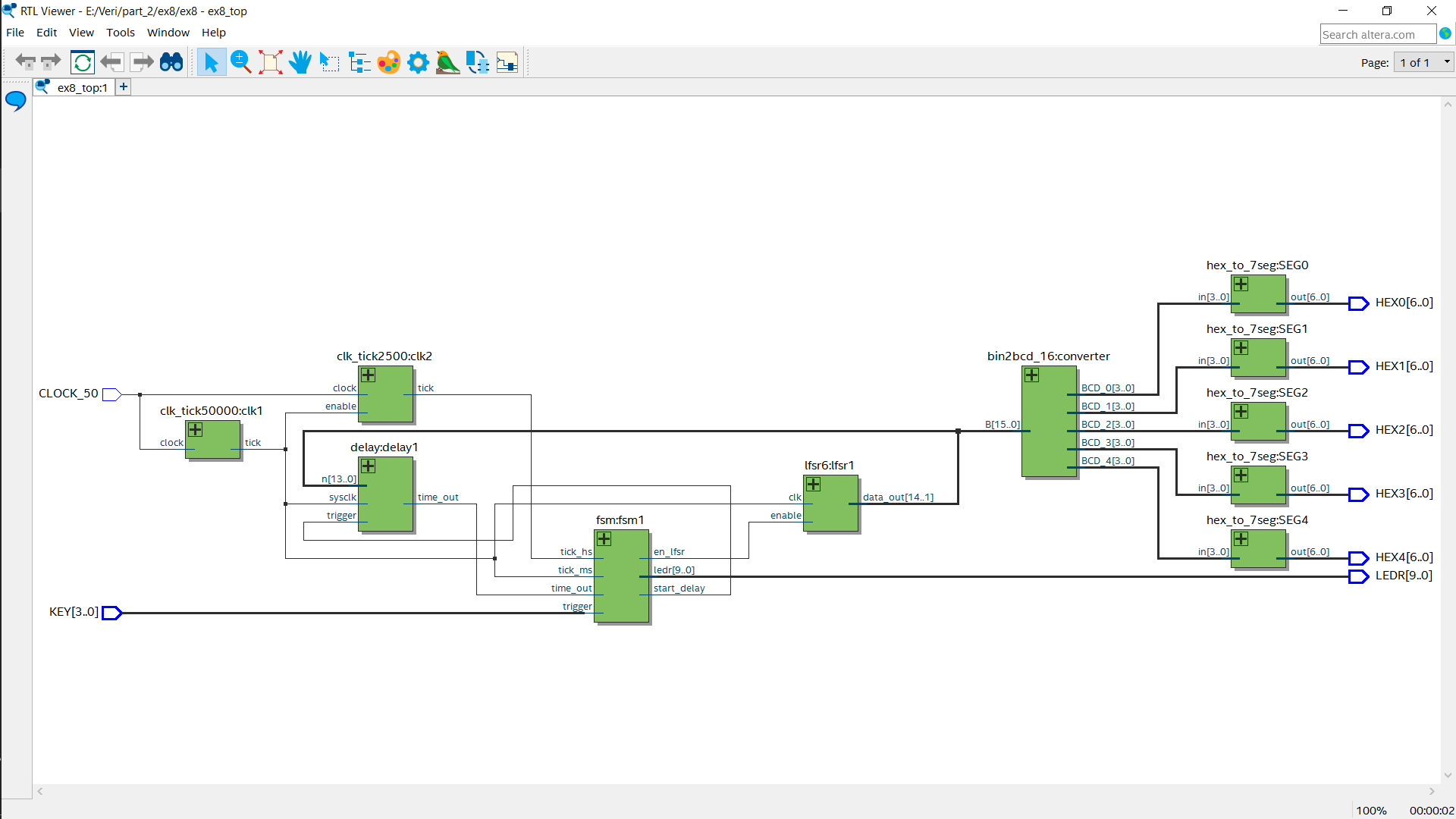
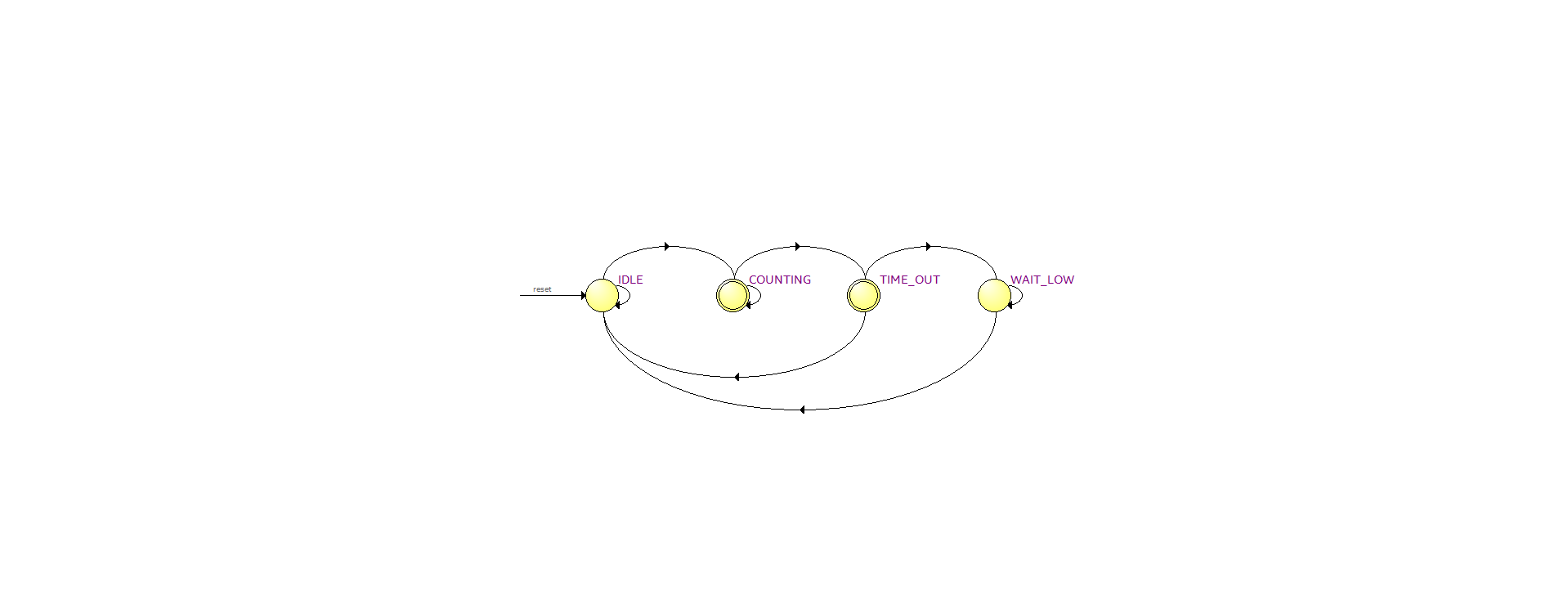
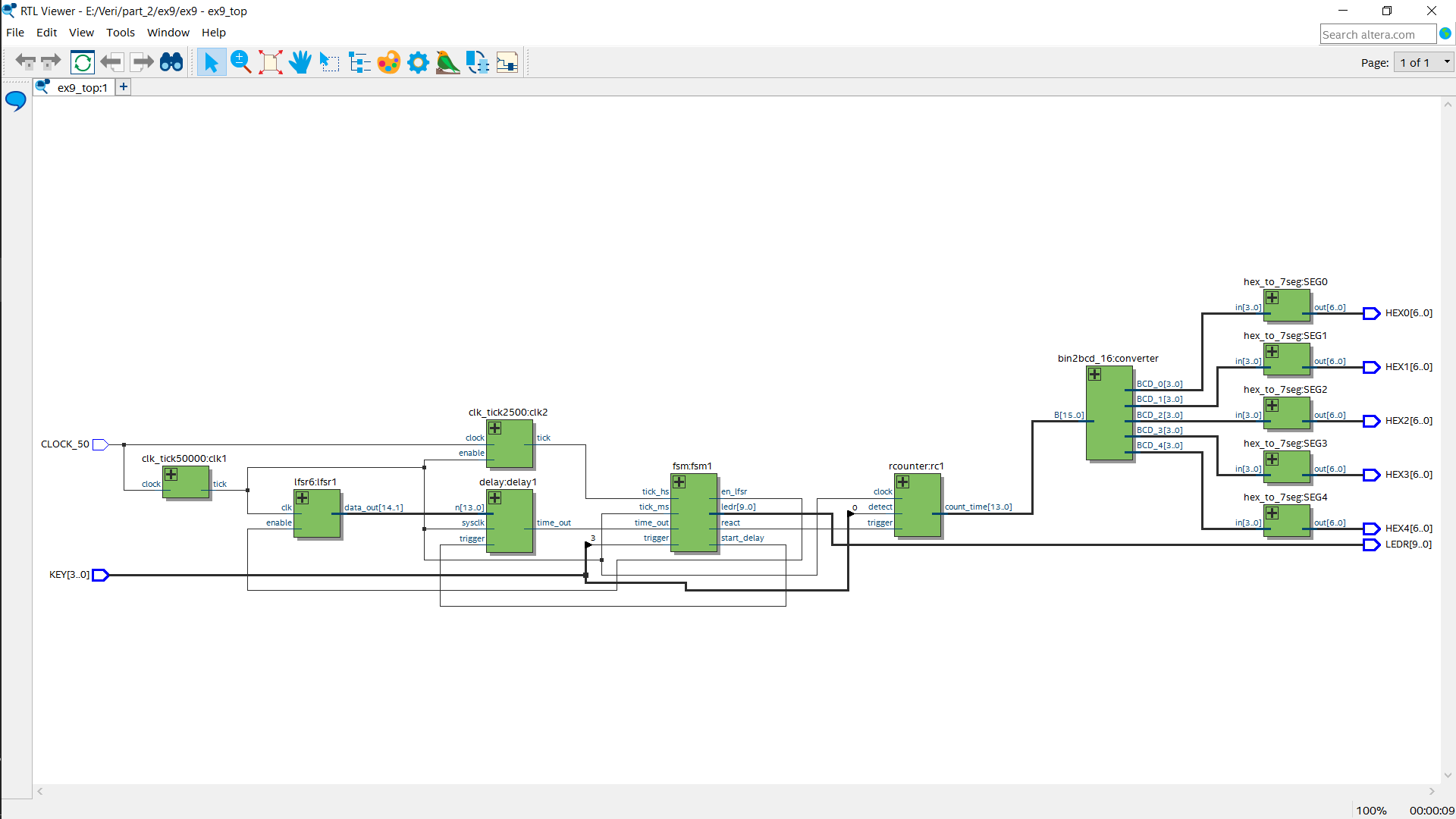
Unconstrained ports - Unconstrained paths are paths without any timing constraints specified to them, i.e. set\_input\_delay, create\_clock, etc. The report details the type of unconstrained paths: clocks, input ports, outputs ports. Altera recommends that all paths and ports be constrained to achieve optimal placement and fitting results. The following example shows the command to generate an unconstrained path report.



Experiment 7





Experiment 8 & 9 (Optional)